PWM and PFM Operation of DC/DC Converters for Portable Applications

Upal Sengupta

ABSTRACT

This topic discusses the trade-offs between fixed-frequency pulse-width modulation (PWM) and pulse-frequency modulation (PFM) for portable DC/DC converter applications. PWM converters offer the benefit of predictable operating frequency, which may simplify the design of circuitry that suppresses electromagnetic interference (EMI). They also offer low output ripple characteristics and high efficiency during moderate- to high-load conditions. However, PWM converters suffer from very poor conversion efficiency at light-load or standby conditions.

PFM or "power-save" operating modes used with PWM converters offer a solution to this problem. Hysteretic or PFM architectures can also offer other benefits for boost converters. Because no loop compensation is required, the converter circuits are relatively simple and easy to design. Under the operating constraints of a typical battery-operated system, the resulting frequency range of a PFM converter may be narrow enough to allow its use even in some relatively noise-sensitive environments.

PFM converters may not be appropriate for all applications. By understanding some basic details regarding the differences between PWM and PFM approaches, the system designer can make a more intelligent choice regarding the best architecture for a particular application.

I. INTRODUCTION

Switch-mode PWM and PFM power converters are commonly used in portable devices to maximize battery life. They provide high efficiency in step-down applications and can also convert the low battery voltage to the higher levels required for LED backlights and display bias.

One of the concerns with switch-mode power converters is the generation of unwanted EMI. PWM converters are often preferred by system designers because they operate at a specified known frequency, which may make the EMI-filtering design process easier. PFM converters inherently have a variable operating frequency, and therefore many system designers have concerns about using this type of architecture in portable products with sensitive audio or RF subsystems.

The concerns associated with the use of variable-frequency-converter architectures are valid ones and should not be dismissed. However, the use of pulse-skipping or PFM architectures can offer significant performance improvement in certain applications. These improvements include better low-power conversion efficiency, lower total solution cost, and simple converter topologies that do not require control-loop-compensation networks.

Understanding variable-frequency operating modes can help the system designer know when it may be beneficial to use a PWM, PFM, or dual-mode architecture for the converter circuit. The terms "PWM" and "PFM" are also sometimes used to describe other aspects of the converter circuit that will be discussed further in the following definitions.

II. BASIC DEFINITIONS

The remainder of this topic assumes that the reader has a basic understanding of DC/DC converters. For further information on the fundamentals, please see References [1], [2], and [3].

A. PWM Converter

A PWM converter is a DC/DC power-converter architecture that uses a fixed-frequency oscillator to drive the power switches and transfer energy from the input to the output. The drive

signal used is constant in frequency but varies in its duty cycle (ratio of power-FET on time to the total switching period). The clock frequency is fixed and the pulse width of each clock cycle is adjusted based on operating conditions. Hence, this approach is referred to as "pulse-width modulation," or "PWM."

B. PFM Converter

A PFM converter is an alternative DC/DC power-converter architecture that uses a variable-frequency clock to drive the power switches and transfer energy from the input to the output. Because the drive signal's frequency is directly controlled to regulate the output voltage, this architecture is referred to as "pulse-frequency modulation," or "PFM." DC/DC converters with constant-on-time or constant-off-time control are typical examples of the PFM architecture.

C. Hysteretic Converter

A hysteretic converter is a simple method for control of a DC/DC conversion circuit in which the power FET is turned on and off based on the output-voltage changes sensed by the converter. This architecture is sometimes also referred to as a "ripple regulator" or "bang-bang controller" because it continuously shuttles the output voltage back and forth to just above or below the ideal setpoint. As in most comparator-based circuits, hysteresis is used to maintain predictable operation and to avoid switch chatter. Because the hysteretic architecture varies the drive signal to the power FETs based on the operating conditions of the circuit, the switching frequency is not constant. The hysteretic approach is therefore one type of PFM architecture.

D. Pulse-Skipping/"Power-Save" Mode

This is a secondary control mode used with some PWM-converter architectures especially for portable or low-power applications. When a PWM converter operates at moderate- to high-load currents, it runs in continuous conduction mode. As the load current decreases, the converter may switch to discontinuous mode. At very light loads, the converter goes into pulse-skipping or power-save mode by intermittently turning off the internal oscillator and re-enabling it only as needed to maintain the output regulation. Because this further "modulates" the switching frequency, this mode of operation is also sometimes referred to as "PFM mode." It does not necessarily mean that the fundamental operation of the converter uses the PFM architecture.

E. LED Brightness Control

The brightness of an LED backlight is typically controlled by setting the current through the LED string. Typical levels used in portable devices are 20 to 25 mA for higher brightness or 5 to 10 mA for lower brightness. Low-power modes may use average currents of 1 mA or less.

F. Analog Dimming

LED brightness can also be controlled by directly changing the continuous current through the LED. The TPS61060 family of devices implements a "digital-dimming" feature that allows a host processor to digitally control LED brightness by sending a command to the IC. The digital command from the processor actually sets an analog feedback voltage within the IC and controls brightness without the need for PWM enable/disable control. Analog dimming can also be applied to most common LED drivers by simply varying the value of an external resistor. Analog dimming may be preferred for very noise-sensitive applications. However, for some types of LEDs, the LED illumination color varies slightly with changes in bias-current that can result in some color shift as the brightness is decreased.

G. PWM Dimming

PWM dimming is a method of controlling LED brightness by turning the LED current on and off at a rate faster than noticeable by the human eye. The converter used to drive the LED string is turned on and off at a rate typically ranging from around 100 Hz up to a few kilohertz. When the converter is on, the current flowing through the LEDs is always the same, which prevents the perception of a color shift in the LEDs. By varying the duty cycle (hence PWM) of the dimming control signal, the average current and thus the perceived brightness of the LED backlight can be precisely controlled.

The term "PWM" in this particular case refers to the modulation of the enable signal to the converter IC, which turns the LED driver on and off as required to set a specific average brightness. The PWM dimming frequency is typically in the range of around 100 Hz to several kilohertz. It should not be confused with the switching frequency of the converter itself, which is typically in the range of hundreds of kilohertz to a few megahertz. PWM dimming may be used with either PWM- or PFM-converter architectures. Fig. 1 illustrates a 50% PWM dimming control applied to the TPS61042 boost converter.

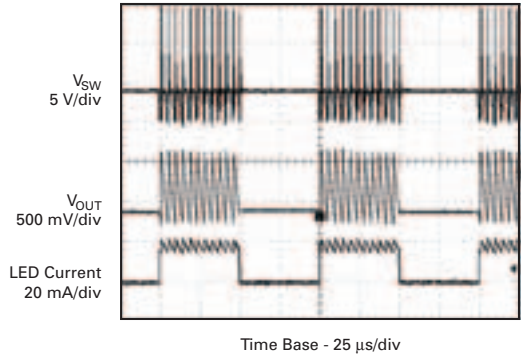


Fig. 1. Typical switching waveforms of TPS61042 converter (4-LED string).

From the switch voltage (V_{SW}) trace, it can be seen that the converter itself completes 11 switching cycles within 50 µs. Thus, the actual switching frequency of the converter under these conditions is approximately

$$f_{SW} = \frac{11}{50 \cdot 10^{-6}} = 220 \text{ kHz}.$$

The converter is turned on for 50 µs and off for 50 µs; in other words, the PWM dimming frequency is 10 kHz with a duty cycle of 50%. When the converter is on, it generates an average LED current of approximately 20 mA. Since the duty cycle is 50%, the long-term, average LED current over multiple cycles is 10 mA. The visible brightness of this LED backlight would appear approximately the same as if it were operated at a constant 10-mA drive current.

H. Switch-Mode-Converter Operating Losses

There are several types of switch-mode-converter loss. "Loss" in this case refers to any area in which energy is drawn from the input without correspondingly being transferred to the output. An ideal converter operates at 100% efficiency and has zero loss. For the purposes of this topic, four types of loss are considered:

- **MOSFET dynamic losses**—These can be divided into gate-drive and switching losses. Gate-drive losses are caused by the energy used to charge and discharge the MOSFET's gate capacitance, and are highest when the FETs are quickly turned on and off at high frequency. Switching losses occur as the MOSFET transitions through its linear operating range, and current flows through the drain-source channel while there is significant drain-source differential voltage. An ideal MOSFET would have zero gate capacitance and infinitely fast switching time, resulting in no switching losses.
- **MOSFET conduction losses**—These are primarily ohmic losses caused by passing high currents through the nonzero channel resistance of the power-switching elements. An ideal MOSFET would have zero on resistance, resulting in no conduction losses.
- **Passive component losses**—For inductors, these can take the form of conduction (wire/winding) losses or magnetic core losses. For capacitors, losses are typically associated with the equivalent series resistance (ESR) of the component and are determined by the choice of external component, operating frequency, and load current.
- **Converter IC losses**—These are from the amount of energy required to operate the power-converter IC itself. These losses include internal bias currents for amplifiers, comparators, and references, but they are typically dominated by the internal oscillator and drive circuits for most PWM converters.

During relatively high-load conditions, the loss associated with converter ICs is relatively small compared to the other types of losses from switch-mode converters. However, as the load current decreases, especially in very light-load or standby conditions, the losses associated with

MOSFET conduction and passive components diminish toward zero while MOSFET dynamic losses and converter-IC losses remain relatively constant for a PWM converter. Thus, at very light loads, the ability to reduce the converter's quiescent current as well as the gate-drive loss is a significant factor in maintaining high efficiency. Reducing the switching frequency under light-load conditions can accomplish both of these goals. There are numerous articles and textbooks that give a more complete treatment of efficiency analysis and sources of loss for switch-mode converters. Refer to References [1], [2], and [3] for additional information.

III. Dual-Mode Buck-Converter Architecture

One of the characteristics of an ideal switch-mode converter is that it provides high efficiency under all operating conditions. In practice, however, this may become very difficult in a portable product that operates across a wide range of load currents. Many portable applications have operating modes such as low-power or "sleep" modes in addition to high-current, fully on operating modes. A typical handheld device may draw 1 mA or less of load current in sleep or standby mode while drawing over 1 A in its maximum-performance operating condition. The classical fixed-frequency, or PWM, operating mode offers good performance under most operating conditions. However, the basic operation of the power-converter IC in this mode usually draws some measurable amount of current ranging up to a few milliamps. If the converter's load (a subsystem such as a microprocessor or memory) is drawing more than 100 mA, then the current drawn by the converter itself may not significantly affect the total efficiency of the power-conversion process. However, as the system load decreases (for example, in standby or low-power operation), the conversion efficiency can decrease significantly because the converter's quiescent current becomes a significant portion of the total current drawn.

To improve efficiency at light-load operation, the operating current of the converter circuit must be reduced. A PWM converter requires an internal oscillator circuit. If the oscillator is always on, it will allow fast transient response to input and load variations. However, this oscillator is one of the main sources of current consumption within the IC. Shutting down the oscillator and some of the internal drive circuitry inside the converter IC can save an appreciable amount of operating current. Under light-load conditions, a pulse-skipping technique (power-save or PFM mode) is used. Power-save mode is entered when the inductor current (sensed within the IC) falls below a predefined threshold. In this mode of operation, the converter switches current from the input to the load only as often as needed to prevent the output from falling out of regulation.

There are some performance trade-offs when using the power-save mode. The transient response of the converter may be slower and the output voltage ripple may be higher. Some increase in output ripple is observed because of the tolerance band used to sense when the power switches need to be turned on again. If a narrower tolerance band is used, the converter switches more frequently, which reduces the benefit of the power-save mode. Thus, there is a direct trade-off between improving low-power efficiency and increased output ripple in power-save mode.

Selectively disabling the oscillator circuit and pulsing the power switches only as needed to maintain regulation can reduce the quiescent current of the IC from a few milliamperes down to several microamperes. The resulting improvement in efficiency can be seen at light loads in Fig. 2.

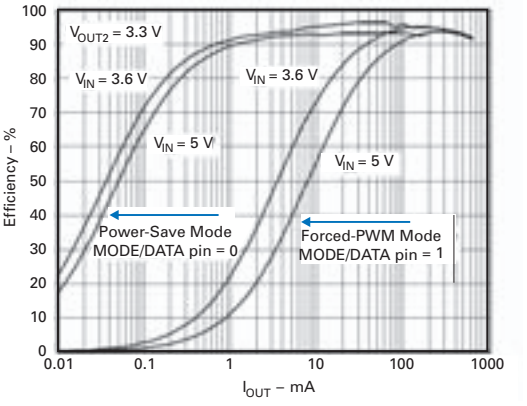


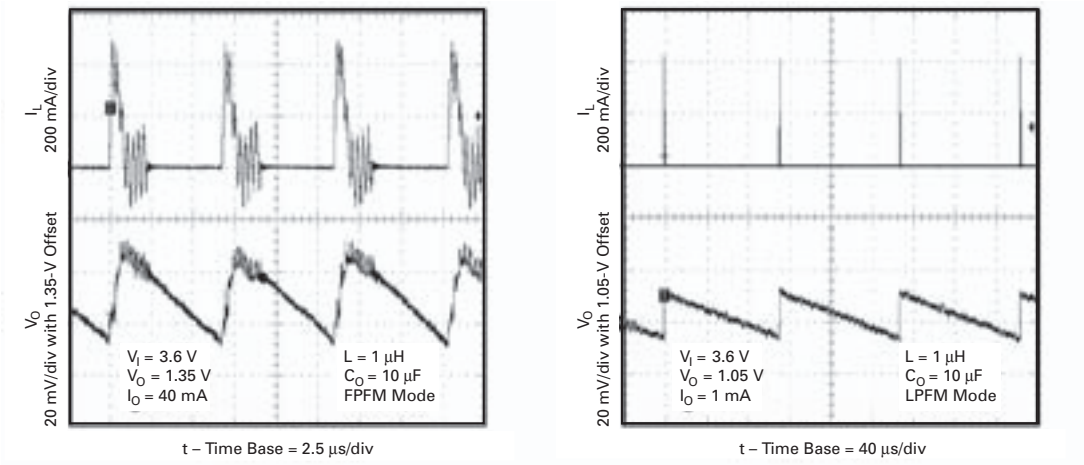
Fig. 2. TPS62400 conversion efficiency for PWM and power-save modes.

This figure illustrates the power-conversion efficiency of the TPS62400 DC/DC converter when it operates in fixed-frequency PWM mode as well as in power-save (PFM) mode at light-load levels. While a fixed-frequency PWM mode can maintain good efficiency above 100 mA, the use of a pulse-skipping PFM mode will allow for converter efficiency in the range of 80 to 90% even at load currents below 1 mA. If the converter was left in PWM mode at this light-load level, its own operating current would be significantly higher than the load current, resulting in very poor conversion efficiency (well under 30%, as shown).

Under very light-load conditions, the converter's output capacitor can maintain the output voltage for some period of time between switching pulses. In the ideal case, the oscillator could be turned completely off at a no-load condition and the output voltage would remain constant due to the charged state of the output capacitor. In reality, of course, some parasitic losses occur, and the circuit requires at least occasional pulsing of the power switches to maintain the output voltage in regulation. Fig. 3 shows pulse skipping of the TPS62350 DC/DC converter at different load conditions. This device has two power-saving modes: the light-load PFM (LPFM) mode and the fast-PFM (FPFM) mode—described in more detail later. It can be seen that the power switch is pulsed more frequently at higher-load levels (FPFM mode). Note that the units on the x and y axes are different for Figs. 3a and 3b. At still higher loads, the converter resumes constant-frequency (PWM-mode) operation with the oscillator fully on.

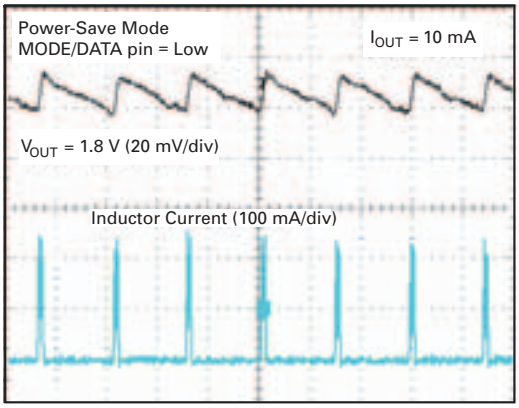
During load transients, any voltage regulator will exhibit some amount of overshoot during a high-to-low load transient or undershoot during a low-to-high load transient. In the case of a converter that has entered power-save mode, the load level is already low, so the next significant load transient that can occur is from low to high current. In an application, this corresponds to "waking up" from sleep mode to active mode, for example. When this occurs, the increased load on the regulator output will result in output-voltage sag until the converter loop has a chance to respond.

To anticipate the output sag that may result in going from a light-load to a high-load operating condition, a technique called "dynamic voltage positioning" is available with the TPS62400. During the power-save mode, the output-voltage setpoint is increased slightly (for example, by 1%) to anticipate the instantaneous negative-going transient that will occur when the load is suddenly stepped higher. This prevents the output voltage from falling below its desired window of regulation during the initial load transient. Details of the voltage positioning technique are provided in the TPS62400 datasheet (see Reference [4]).

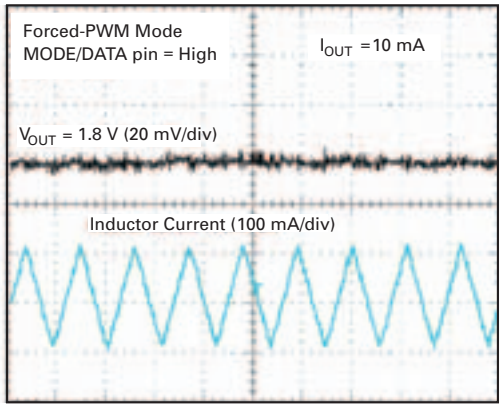


a. Fast-PFM mode with 40-mA load. *b. Light-load PFM mode with 1-mA load.*

Fig. 3. TPS62350 pulse skipping at 40-mA and 1-mA load conditions.



a. Light-load V_{OUT} ripple in power-save mode.



b. V_{OUT} ripple in forced-PWM mode.

Fig. 4. TPS62401 power-save (PFM) and fixed-frequency (PWM) operation waveforms.

Fig. 4a shows the increased output-voltage ripple and periodic switching cycles that occur in the power-save mode at light loads; it also shows the slightly higher output-voltage setpoint. Fig. 4b shows the reduced ripple voltage and continuous switching cycles that occur when the converter is operated in the forced-PWM mode.

An additional enhancement that can be implemented to balance the trade-off between good transient response (best in PWM mode) and low power consumption (best in power-save/LPFM mode) is an intermediate or FPFM mode as shown for the TPS62350 in Fig. 5. The user can control the mode of operation using I^2C commands to the converter IC. The device will automatically transition between either the LPFM or the FPFM power-save mode (based on its preprogrammed register configuration) and the PWM mode as required by the load-current level.

The LPFM mode works well for a system that goes from a high load to a very light load, as in sleep-mode operation. The LPFM control scheme is based on a fixed inductor peak current. To get a proper automatic transition between LPFM and PWM operation, the inductor peak current is set higher than the PWM peak-to-peak ripple current. During the pulse-skipping phase, the converter runs only its internal reference and a comparator to monitor the output voltage. The advantage of LPFM is much lower quiescent current and higher efficiency compared with FPFM at low output loads.

If appropriately configured, the TPS62350 will automatically transition from PWM mode into FPFM mode when the following conditions are met simultaneously for three or more clock cycles:

- The output voltage is within its regulation limits.
- The inductor valley current reaches zero.

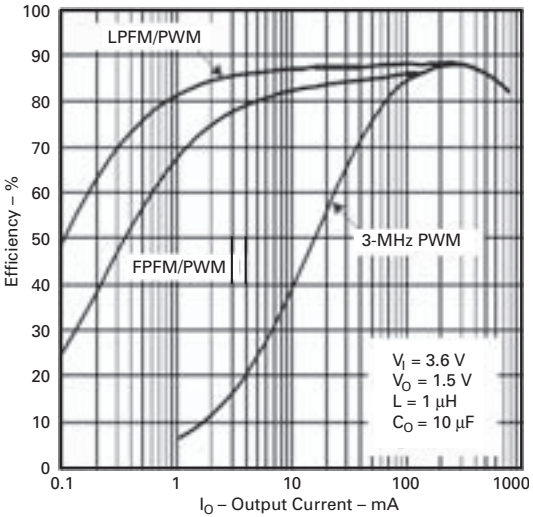


Fig. 5. LPFM, FPFM, and fixed-frequency PWM efficiency of TPS62350.

In FPFM mode, the converter ramps up the output voltage by means of its PWM control loop. This typically requires several switching cycles. Once the output voltage falls below the nominal low-voltage threshold, the PMOS switch is turned on and the device exits power-save mode. During PFM operation, the TPS62350 converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load.

TI components that support the power-save mode also provide a logic input that, if required by the application, allows the converter to be operated in forced-PWM mode regardless of the load condition. This is useful when the fast transient response and other performance characteristics of the PWM mode are more important than conversion efficiency for specific operating modes. If the forced-PWM mode is not asserted, the device will auto-switch between PWM and power-save/PFM modes as required by the load-current level.

IV. Fixed-Frequency and Hysteretic Boost Converters

The application of a fixed-frequency control architecture provides the same benefits for boost-converter circuits as for buck-converter circuits. The fixed operating frequency allows for predictable design of EMI-filtering components, but variable-frequency-converter architecture can offer many benefits in boost applications.

Fig. 6 is a block diagram of the TPS61020 PWM-mode boost converter. Like the converters previously discussed, the TPS61020 has a power-save mode for light-load currents, so it can operate as a variable-frequency device under some load conditions.

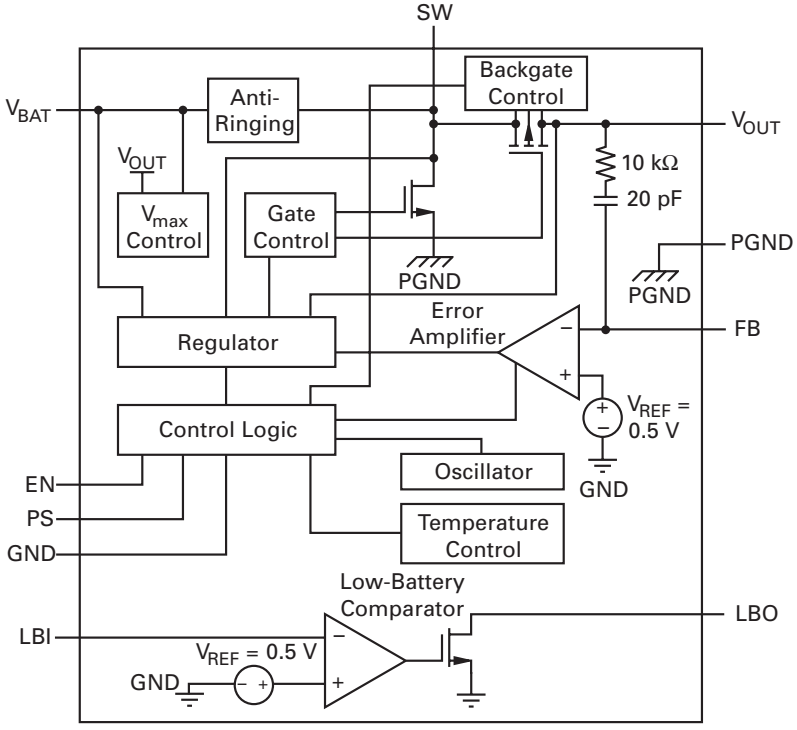


Fig. 6. Functional block diagram of TPS61020 boost converter.

Fig. 7 is a block diagram of the TPS61042 boost converter. Note that this device does not have an internal oscillator. As discussed earlier, a conventional PWM converter uses its clock to generate a drive signal to the power FETs. (This drive signal may be gated off or further controlled by several other factors, as described in the references listed at the end of this topic.)

The TPS61042 shown in Fig. 7 uses hysteretic-converter architecture that operates in a different manner. As previously mentioned, this architecture is sometimes called a "bang-bang controller." In this circuit, the main power switch, Q1, is turned on until a fixed peak current is reached. When the switch is turned on, the inductor current begins to increase. The ramp time to reach the peak threshold limit is dependent on the inductor value, L, and the other operating conditions of the circuit. Once the peak current is reached, the switch is turned off and the energy is transferred to the output as in any boost converter. The switch is turned on again when the feedback pin (FB), or sense voltage, falls below the internal reference point.

This type of converter therefore essentially self-oscillates based on the measurement of the FB voltage and the internal switch current. The power FET is turned on when required (i.e., when the FB voltage has fallen below the limit, typically 250 mV) and then turned off when the internal peak current has reached the upper limit (typically 500 mA). Because the FB voltage is affected by the load conditions, and the ramp time is affected by the inductor value and the input voltage, it follows that the effective frequency of oscillation will be a function of all of these parameters.

This architecture inherently results in some small amount of ripple in the output voltage, since the power FET is controlled based on FB sagging below the reference. For applications such as LED backlight drivers, a small amount of ripple does not visibly affect the LED brightness. For applications that require very low-ripple output voltages, a second-stage filter or linear post-regulator (LDO) is sometimes used after the output section of a hysteretic converter.

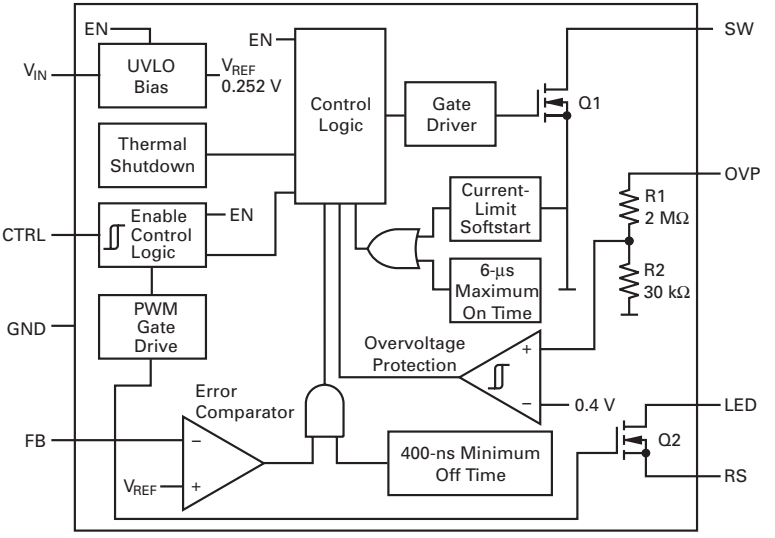


Fig. 7. Functional block diagram of TPS61042 boost converter.

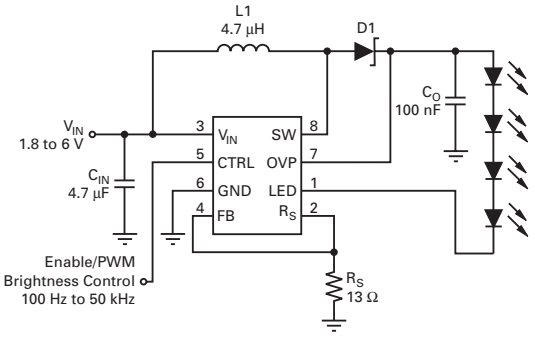


Fig. 8. Typical TPS61042 boost-converter application.

In Fig. 8, the TPS61042 is optimized for LED-driver applications; and the FB voltage from the sense resistor, R_S, is typically used to monitor the current flowing through the LEDs. However, if desired, the designer can easily modify the circuit to generate a constant-voltage output by using an external high-impedance feedback divider to generate the FB signal (see Reference [5]).

In the Fig. 8 example, the peak inductor current during a switching cycle is given by the equation

$$I_{PK} = I_{LIM} + \frac{V_{IN}}{L} \bullet 100\ ns,$$

where I_{LIM} is the internal switch-current limit (typically 500 mA for the TPS61042), and V_{IN} is the input battery voltage. The operating switching frequency (f_{SW}) of the TPS61042 converter is given by

$$f_{SW} = \frac{2I_{LOAD} \bullet (V_{OUT} - V_{IN} + V_{DIODE})}{L \bullet I_{PK}^2},$$

where I_{LOAD} is the current through the LED string (20 mA in the example), V_{OUT} is the voltage across the LED string and R_S (approximately 13.5 V for the four-LED example, or around 20 V for a six-LED string), and V_{DIODE} is the forward voltage drop of the external rectifier (typically 0.4 V). The switching frequency is affected by load current, input and output voltage, the internal switch-current limit, and the inductor value. Since a nonideal rectifier diode is used, its forward loss must also be considered.

The switching frequency can vary over a wide range (<100 kHz to 1 MHz) if all variations in operating conditions are considered. However, for the typical LED backlight application in a portable product, in practice there are several factors that constrain the range of frequencies that occur. For example, the input voltage (from the battery or an external adapter) typically varies over only a finite range such as 3.0 to 5.0 V. Furthermore, the LED string itself is often operated at a fixed brightness when on. To maintain consistent LED color in variable-brightness displays, changing the continuous bias current is discarded in favor of using PWM dimming to actually pulse the display on and off. Thus, the actual load that the converter is driving when it is on does not vary significantly.

Fig. 9 shows the calculated variation in operating frequency for a TPS61042 used to generate a 13.35-V output (corresponding to four LEDs in series at 20.5-mA drive current) for a typical range of input voltage. The three different traces show results for inductance values of 2.2, 3.3, and 4.7 µH. Actual measured frequency at specific voltages for the TPS61042 EVM driving four LEDs at 20.5 mA and using a nominal 4.7-µH inductor is marked on the graph for comparison.

So, for a hysteretic boost converter used across a fixed range of input voltage and load current, the operating frequency range can be predicted, and EMI-filter components can be selected accordingly if needed. Furthermore, the hysteretic-converter architecture does not require

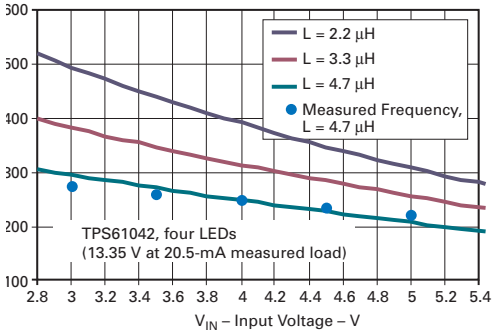


Fig. 9. Variation in TPS61042 calculated and measured switching frequency.

control-loop compensation. Thus it can operate well with a wide range of inductor values and a relatively small output capacitor, particularly in applications where the voltage ripple is not extremely critical, such as in WLED drivers. The effective operating frequency can also be adjusted higher or lower by choosing the L value if desired.

V. Summary and Conclusion

The basic operational differences between PWM and PFM architectures have been reviewed. In practice, some designers of portable systems try to avoid designs with variable-frequency converters because of the concern about EMI or other aspects related to variable-frequency operation. In some cases, these concerns are valid due to the interaction of PFM converters with sensitive subsystems elsewhere in the portable product. However, PFM architecture offers some real benefits:

- Better efficiency at light-load conditions.
- Better efficiency across a wide range of LED bias currents for boost converters.
- Stable, easy-to-implement converter designs that allow for the use of a wide range of inductor components.

Concerns regarding EMI can sometimes be reduced:

- In the buck-converter application, the circuits illustrated operate using fixed-frequency PWM under high-power conditions.
- When the circuits enter variable-frequency power-save mode, the total output-power levels are very low.
- Because the root cause of EMI is fast switching of high currents and high voltages, variable-frequency operation is not usually a concern in low-power modes.
- Generating WLED backlight is a primary application of boost converters in portable applications.
- In WLED backlights, in many cases the circuit is operated at relatively fixed output-current levels with a relatively narrow range of input-voltage variation.
- If needed, these converters can be set to forced-PWM mode if transient response or other considerations are more important than conversion efficiency in specific operating modes of a given portable system.
- It is possible to determine and test the range of frequency variation that is likely to be encountered in a real application and, if necessary, to tune the operating frequencies with the choice of an appropriate inductor value.

However, if it is determined that the variable-frequency operating range is too wide for a sensitive application, the system designer should consider the use of fixed-frequency PWM architecture rather than a hysteretic PFM design. In some cases, the compromise may be a trade-off between efficiency and low-noise operation. As with many engineering problems, there is no single best answer but a range of application-specific issues that need to be considered.

VI. References

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